PROCESS FOR FORMING LOW RESISTANCE CONTACTS BETWEEN SILICIDE AREAS AND UPPER LEVEL POLYSILICON INTERCONNECTS

This application is a continuation of application Ser. No 07/713,589 filed Jun. 6, 1991, now abandoned.

FIELD OF THE INVENTION

This invention relates to semiconductor devices and more particularly to a CMOS process to fabricate low resistive contacts between silicide areas and an upper level of polysilicon.

BACKGROUND OF THE INVENTION

During the fabrication of semiconductor devices using CMOS technology, conductive interconnects (or contacts) between different types of conductive material are required to form a circuit. For example, as an MOS transistor is formed in a silicon substrate's active area, its' gate, source and drain then have to be connected to other circuitry by a conductor, such as a conductively doped polysilicon line.

These interconnects are typically formed by depositing a layer of polysilicon over a desired buried contact location thus allowing the polysilicon to fill the contact hole and make physical connection to the underlying active area. Next the polysilicon is doped by a doping source to make an electrical connection. However, as critical dimensions became smaller, which shrinks the contact opening, a low resistive contact becomes very difficult if not impossible to obtain.

Several methods to form low resistive contact structures in MOS devices have been investigated that include: self-aligned silicides on the source/drain regions, elevated source/drain regions, buried-oxide MOS contacts and selectively deposited layers of metal in the contact holes. The most attractive approach turns out to be the self-aligned silicides on the source/drain regions as this self-aligned process does not entail any additional masking steps over a conventional contact formation process.

A typical process for forming self-aligned silicide contacts to an MOS transistor is shown in FIGS. **1***a*–**1***e*. FIG. **1***a* shows previously doped active areas **2** (see FIG. **1***a*) implanted into silicon substrate **1** to form the transistor's source and drain. Oxide **3**, separates substrate **1** from a polysilicon gate structure **4** to form the transistor's gate oxide.

In FIG. **1***b*, oxide **3** has been etched and silicon dioxide spacers **5** are deposited and etched. In FIGS. **1***c* and **1***d*, a metal has been deposited and annealed to form metal silicide **6**, followed by selectively removing the unreacted metal.

Finally, in FIG. **1***e*, dielectric **7** is deposited and contact holes are opened down to silicide **6**. Now metal **8** is deposited into the contact holes to make contact with silicide **6**.

The typical approach to develop self-aligned silicide contacts provides good ohmic contacts between a source/drain active area and an upper lying conductor. Unfortunately, the upper lying conductor must be formed from a metal while polysilicon cannot be used as effectively without reintroducing the problems of a high resistive contact of conventional buried contacts.

The present invention introduces a process that further develops the use of silicide contacts and in particular self aligned silicide (or salicide) contacts, by developing a doping scheme that will allow the use of an upper layer of polysilicon as the interconnect layer between a silicided conductor while maintaining a low resistive contact.

SUMMARY OF THE INVENTION

The invention is directed to a process for forming low resistive contact between silicide areas and upper level polysilicon interconnect layers. A specific doping technique is developed that provides solid low resistive contacts between a lower level of a silicided area and an upper level polysilicon interconnect. The doping technique combines the doping implant of the upper level polysilicon and an ion-mixing implant into a single implant thereby achieving said low resistive implant which also reduces processing steps.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a*–**1***e*, illustrate a typical process for forming self-aligned silicide contact structures on a MOS transistor;

FIG. **2** shows a cross-sectional view of an in process wafer portion having source/drain regions implanted into a silicon substrate for a MOS transistor, a transistor gate and gate oxidation, and a conductor separated from the silicon substrate by field oxide;

FIG. **3** shows a cross-sectional view of the in-process wafer portion of FIG. **2** after a conformal deposition of metal;

FIG. **4** shows a cross-sectional view of the in-process wafer portion of FIG. **3** after an annealing step to form metal silicide on conductive material followed by an etch to remove unreacted metal;

FIG. **5** shows a cross-sectional view of the in-process wafer portion of FIG. **4** after a conformal deposition of oxide followed by a contact etch to provide access to the desired interconnects yet to be made;

FIG. **6***a* shows a cross-sectional view of the in-process wafer portion of FIG. **4** after a conformal deposition of polysilicon followed by a doping impurities implant to form low resistive contacts between the desired silicided areas and the upper level polysilicon;

FIG. **6***b* represents a dopant profile resulting from the implant step of FIG. **6***a*; and

FIG. **7** shows a cross-sectional view of the in-process wafer portion of FIG. **6***a* after patterning and etching of the upper level of polysilicon.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is directed to a process for forming low resistive contacts between lower level silicided areas and upper level polysilicon interconnect layers. A specific doping technique process is developed in a sequence shown in FIGS. **2**–**7**.

As shown in FIG. **2**, a silicon wafer is fabricated using conventional process steps, known to one skilled in the art, up to the point of having formed source/drain regions **22** in silicon substrate **21**, conductive transistor gate **23** and gate oxidation **24**, and conductor **25** separated from silicon substrate **21** by field oxidation **26**.

Referring now to FIG. **3**, a layer of metal **31**, such as, Titanium (Ti), Cobalt (Co), Platinum (Pt), Tungsten (W), Molybdenum, Palladium or Tantalum, is placed over the existing wafer surface. This metal is preferably deposited by chemical vapor deposition (CVD), however it could also be sputtered on or placed by any other conventional means available.